What is claimed is:

1. A frequency prescaler comprising:

a first sequential element having an input stage with at least one embedded logic gate; and

a second sequential element having a clock input node coupled to an output node of the first sequential element.

2. The frequency prescaler of claim 1 wherein the first sequential element is coupled to perform a conditional divide-by-two operation.

3. The frequency prescaler of claim 1 further comprising a third sequential element, and wherein the at least one logic gate is coupled to receive a signal from the output node of the first sequential element and is coupled to receive a signal from the third sequential element.

4. The frequency prescaler of claim 3 wherein the third sequential element is coupled to decode a state of the first and second sequential elements.

5. The frequency prescaler of claim 4 wherein the third sequential element includes at least one logic gate embedded within an input stage.

6. The frequency prescaler of claim 1 wherein the first sequential element comprises a true single phase clock flip-flop.

7. The frequency prescaler of claim 1 wherein:

the first sequential element includes a clock input node configured to receive a voltage controlled oscillator output signal; and

the first and second sequential elements are configured to form an asynchronous counter.

8. The frequency prescaler of claim 7 further comprising a third sequential element having an output node coupled to an input node of the at least one logic gate of the first sequential element, and configured to decode a state of the asynchronous counter.

9. The frequency prescaler of claim 8 wherein the third sequential element is configured to be responsive to a control signal to conditionally lengthen a period of the asynchronous counter by one cycle of the voltage controlled oscillator output signal.

10. The frequency prescaler of claim 9 wherein the first sequential element comprises a true single phase clock flip-flop.

11. The frequency prescaler of claim 9 wherein the third sequential element comprises a true single phase clock flip-flop having an input stage with an embedded logic gate.

12. An even/odd modulus prescaler comprising:

an asynchronous counter having a least significant stage clocked by an input signal; and

a first true single phase clock flip-flop having an input stage with an embedded logic gate to decode a state of the asynchronous counter, configured to modify a modulus of the asynchronous counter between an even modulus and an odd modulus.

13. The even/odd modulus prescaler of claim 12 wherein the least significant stage of the asynchronous counter comprises a second true single phase clock flip-flop having an input stage with an embedded logic gate.

14. The even/odd modulus prescaler of claim 13 wherein the embedded logic gate of the least significant stage is coupled to receive signals from an output node of the least significant stage and from the first true single phase clock flip-flop.

15. The even/odd modulus prescaler of claim 14 wherein the asynchronous counter further comprises a more significant stage having a clock input node coupled to the output node of the least significant stage.

16. The even/odd modulus prescaler of claim 12 wherein the asynchronous counter comprises at least one additional more significant stage, wherein each of the at least one additional more significant stage is configured to be clocked by a lesser significant stage.

17. A frequency synthesizer comprising:

a comparison circuit to compare a reference signal and a frequency divided signal;

a voltage controlled oscillator to synthesize an output signal in response to the comparison circuit; and

a prescaler coupled to the voltage controlled oscillator to divide a frequency of the output signal, wherein the prescaler includes an asynchronous divider with at least one true single phase clock flip-flop having embedded logic in an input stage.

18. The frequency synthesizer of claim 17 wherein the at least one true single phase clock flip-flop includes a least significant flip-flop coupled to be clocked by the output signal, the least significant flip-flop including an input stage having an embedded logic gate.

19. The frequency synthesizer of claim 18 wherein the at least one true single phase clock flip-flop further includes a more significant flip-flop coupled to be clocked by a signal produced by the least significant flip-flop.

20. The frequency synthesizer of claim 19 wherein the at least one true single phase clock flip-flop further includes a decoder flip-flop to decode a state of the least significant flip-flop and the more significant flip-flop.

21. The frequency synthesizer of claim 20 wherein the decoder flip-flop comprises a true single phase clock flip-flop having an embedded logic gate to decode the state.

22. The frequency synthesizer of claim 20 wherein the decoder flip-flop is configured to be clocked by the output signal.

23. An electronic system that includes a direct conversion receiver with an oscillator input port, a directional antenna coupled to the direct conversion receiver, and a frequency synthesizer coupled to the oscillator input port, the frequency synthesizer comprising:

a comparison circuit to compare a reference signal and a frequency divided signal;

a voltage controlled oscillator to synthesize an output signal in response to the comparison circuit; and

a prescaler coupled to the voltage controlled oscillator to divide a frequency of the output signal, wherein the prescaler includes an asynchronous divider with at least one true single phase clock flip-flop having embedded logic in an input stage.

24. The electronic system of claim 23 wherein the at least one true single phase clock flip-flop includes a least significant flip-flop coupled to be clocked by the output signal, the least significant flip-flop including an input stage having an embedded logic gate.

25. The electronic system of claim 24 wherein the at least one true single phase clock flip-flop further includes a more significant flip-flop coupled to be clocked by a signal produced by the least significant flip-flop.

26. A method comprising:

clocking a first sequential element with an input signal, wherein the first sequential element comprises a true single phase clock flip-flop;

clocking a second sequential element with an output signal from the first sequential element;

decoding a state of the first and second sequential elements; and

conditionally gating an input signal to the first sequential element using a logic gate embedded in an input stage of the true single phase clock flip-flop.

27. The method of claim 26 wherein decoding comprises receiving output signals from the first and second sequential elements at a logic gate embedded in an input stage of a third sequential element.

28. The method of claim 27 further comprising clocking the third sequential element with the input signal.

29. The method of claim 26 wherein clocking a first sequential element with an input signal comprises clocking the first sequential element with a voltage controlled oscillator output signal.